CLAIMS

What is claimed is:

1. A semiconductor package with a heat sink, comprising:

a chip carrier;

at least one chip mounted on the chip carrier and electrically connected to the chip carrier;

a heat sink having a first surface, a second surface opposing the first surface, and a plurality of side surfaces interconnecting the first surface and the second surface, wherein the first surface is attached to the chip for interposing the chip between the chip carrier and the heat sink, and the second surface is formed with an interface layer thereon, while adhesion between the interface layer and a molding compound being smaller than that between the first surface of the heat sink and the molding compound; and

an encapsulant made of the molding compound for encapsulating the chip and filling a gap between the first surface of the heat sink and the chip carrier, while the interface layer and the side surfaces of the heat sink being exposed to outside of the encapsulant, and the side surfaces of the heat sink being in a coplane with side edges of the encapsulant.

2. The semiconductor package of claim 1, wherein the heat sink has a surface area dimensionally same as that of the chip carrier.
3. The semiconductor package of claim 1, wherein the interface layer on the second surface of the heat sink is made of a material selected from a group consisting of gold, chromium, nickel, alloy thereof or Teflon.
4. The semiconductor package of claim 1, wherein the chip carrier is a substrate.
5. The semiconductor package of claim 4, wherein the chip is electrically connected to the substrate through bonding wires.
6. The semiconductor package of claim 4, wherein the chip is electrically connected to the substrate through solder bumps.
7. The semiconductor package of claim 1, wherein the chip carrier is a QFN (quad flat nonlead) lead frame.
8. The semiconductor package of claim 7, wherein the chip is electrically connected to the QFN lead frame through bonding wires.

9. The semiconductor package of claim 1, wherein the first surface of the heat sink is roughened, corrugated or made uneven.

10. The semiconductor package of claim 1, wherein at a position on the first surface of the heat sink corresponding to the chip there is formed a connecting portion extending toward the chip for connecting the heat sink to the chip through the connecting portion, while the first surface of the heat sink other than the position of the connecting portion being spaced from the chip.

11. The semiconductor package of claim 1, wherein the heat sink is attached to the chip through a thermally conductive adhesive.

12. A semiconductor package with a heat sink, comprising:

a chip carrier;

at least one chip mounted on the chip carrier and electrically connected to the chip carrier;

at least one buffer pad attached to the chip and made of a material having a similar thermal expansion coefficient to the chip;

a heat sink having a first surface, a second surface opposing the first surface, and a plurality of side surfaces interconnecting the first surface and the second surface, wherein the first surface is attached to the buffer pad for interposing the buffer pad between the heat sink and the chip so as to space the first surface from the chip, and the second surface is formed with an interface layer thereon, while adhesion between the interface layer and a molding compound being smaller than that between the first surface of the heat sink and the molding compound; and

an encapsulant made of the molding compound for encapsulating the chip and the buffer pad, and for filling a gap between the first surface of the heat sink and the chip carrier, while the interface layer and the side surfaces of the heat sink being exposed to outside of the encapsulant, and the side surfaces of the heat sink being in a coplane with side edges of the encapsulant.

13. The semiconductor package of claim 12, wherein the heat sink has a surface area dimensionally same as that of the chip carrier.

Sub B4

14. The semiconductor package of claim 12, wherein the interface layer on the second surface of the heat sink is made of a material selected from a group consisting of gold, chromium, nickel, alloy thereof or Teflon.
15. The semiconductor package of claim 12, wherein the chip carrier is a substrate.
16. The semiconductor package of claim 15, wherein the chip is electrically connected to the substrate through bonding wires.
17. The semiconductor package of claim 12, wherein the chip carrier is a QFN (quad flat nonlead) lead frame.
18. The semiconductor package of claim 17, wherein the chip is electrically connected to the QFN lead frame through bonding wires.
19. The semiconductor package of claim 12, wherein the first surface of the heat sink is roughened, corrugated or made uneven.
20. The semiconductor package of claim 12, wherein the heat sink is attached to the buffer pad through a thermally conductive adhesive.